

83. The memory element of claim 79, wherein said  
programmable resistance material comprises a chalcogen  
element.

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Remarks

The Office Action of April 11, 2001 is discussed in detail below. The original claims 1-39 have been cancelled and new claims 44-83 have been added. Support for the new claims is found in the specification and drawings as originally filed.

Claim Rejections - 35 USC 112

Paragraph 2 of Office Action

Claim 14 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Claim 14 has been cancelled. Applicant respectfully requests that the rejection be removed.

Claim Rejection - 35 USC 102

Claims 1-31 and 35-39 are rejected under 35 USC 102(e) as being anticipated by Ovshinsky (US 5,687,112).

Claims 1-31 and 35-39 have been cancelled. Claims 44-83 have been added.

Ovshinsky (5,687,112) is directed to a programmable resistance memory element. Figure 2 of Ovshinsky shows a memory element. Referring to Figure 2, it is seen that the memory element comprises a conductive layer 14, a conductive layer 34 formed on conductive layer 14, and dielectric layer 18 formed on conductive layer 34. Conductive layer 34 is disposed between conductive layer 14 and dielectric layer 18.

This is distinct for applicant's invention as recited in either independent claims 44, 51, 58, 65, 72 and 78.

Applicant's claim 44 recites:

*44. A memory element, comprising:*

***a conductive layer;***

***a first dielectric material and a second dielectric material, at least a portion of said conductive layer disposed between said first and second dielectric materials wherein an edge portion of said conductive layer is exposed; and***

***a programmable resistance material adjacent to said edge portion.***

In applicant's invention as recited in new independent claim 44, the conductive layer is disposed between a first dielectric material and a second dielectric material (see, for example, Figure 1 of applicant's disclosure which shows conductive layer 130a disposed between dielectric materials 140 and 128. In contrast, Ovshinsky teaches conductive layer 34 disposed between another conductive layer 14 and a dielectric layer 18. Hence, Ovshinsky fails to teach or suggest applicant's invention as recited in claim 44. Similar argument holds of new independent claim 51.

Applicant's independent claim 58 recites:

*58. A memory element, comprising:*

***a first dielectric material;***

***a conductive layer disposed on said first dielectric material;***

***a second dielectric material disposed on said conductive layer*** wherein an edge portion of said spacer is exposed; and

*a programmable resistance material adjacent to said edge portion.*

In applicant's invention as recited in independent claim 58, a conductive layer is disposed on a first

dielectric material, and a second dielectric material is disposed on the conductive layer. (see, for example, Figure 1 of applicant's disclosure which shows conductive layer 130b disposed on a dielectric material 128 and dielectric material 140 disposed on conductive layer 130b).

This is distinct from Ovshinsky's Figure 2 which shows a conductive layer 34 formed on another conductive layer 14, and dielectric layer 18 formed on conductive layer 34. Hence, Ovshinsky fails to teach or suggest applicant's invention as recited in claim 58. Similar arguments hold for applicant's claim 65.

Applicant's independent claim 72 recites:

72. A memory element, comprising:

**a first dielectric material having a sidewall surface formed therein;**

**a conductive sidewall spacer disposed on said sidewall surface;**

**a second dielectric material disposed on said conductive sidewall spacer** wherein an edge portion of said spacer is exposed; and

a programmable resistance material adjacent to said edge portion.

Referring again to Figure 2 of Ovshinsky, conductive layer 34 is formed on another conductive layer 14, and dielectric layer 18 is formed on conductive layer 34. This is again distinct from applicant's invention as recited in independent claim 72 where a conductive sidewall spacer is disposed on the sidewall surface of a first dielectric material, and a second dielectric material is disposed on the sidewall spacer. Hence, Ovshinsky also fails to either teach or suggest applicant's invention as recited in independent claim 72. Similar argument holds for claim 78.

Hence, Ovshinsky fails to teach or suggest applicant's invention as recited in either independent claims 44, 51, 58, 65, 72 and 78. Likewise, Ovshinsky fails to teach or suggest the limitations of the corresponding dependent claims. Hence, Ovshinsky fails to teach or suggest applicant's invention as recited in new claims 44-83. The rejection of new claims 44-83 as being anticipated by or obvious under Ovshinsky is thus improper.

Hence, the rejection of claims 1-31 and 35-39 as being anticipated by Ovshinsky is overcome and applicant respectfully requests it be removed.

Paragraph 6

Claims 1-14, 17-18, 20-22, 28-37 and 39 are rejected under 35 USC 102(b) as being anticipated by Ovshinsky et al (US 5,414,271).

Claims 1-14, 17-18, 20-22, 28-37 and 39 have been cancelled. New claims 44-75 have been added.

Ovshinsky (5,414,271) is directed to a programmable resistance memory element. Figure 1 of Ovshinsky teaches the following:

- conductive layer 32 formed on dielectric layer 20,
- conductive layer 34 formed on conductive layer 32,
- memory material layer 36 formed on conductive layer 34.

Hence, conductive layer 32 is between the dielectric layer 20 and another conductive layer 34. This is distinct from applicant's invention as recited in independent claims 44 and 51. Ovshinsky provides no teaching or suggestion of:

***...a conductive layer;***

***a first dielectric material and a second dielectric material, at least a portion of said conductive layer disposed between said first and second dielectric materials...***

as recited by applicant in independent claim 44 and 51.

The teaching of Ovshinsky is also distinct from applicant's invention as recited in claims 58 and 65. That is, Ovshinsky fails to show:

*...a first dielectric material;*

*a conductive layer disposed on said first dielectric material;*

*a second dielectric material disposed on said conductive layer...*

as recited by applicant in independent claims 58 and 65.

Likewise, the teaching of Ovshinsky is distinct from applicant's invention as recited in independent claims 72 and 78. That is, Ovshinsky fails to show:

*...a first dielectric material having a sidewall surface formed therein;*

*a conductive sidewall spacer disposed on said sidewall surface;*

*a second dielectric material disposed on said conductive sidewall spacer...*

as recited by applicant in independent claims 72 and 78.

Ovshinsky fails to teach or suggest all of the limitations of independent claims 44, 51, 58, 65, 72, 78 as

well as the limitations of all corresponding dependent claims. The rejection of new claims 44-83 as being anticipated by or obvious under Ovshinsky is improper.

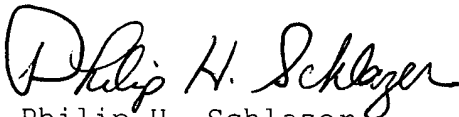
Hence, the rejection of claims 1-14, 17-18, 20-22, 24-26, 28-37 and 39 under 35 USC 102(b) as being anticipated by Ovshinsky et al (US 5,414,271) as been overcome and applicant respectfully requests it be removed.



# **SUMMARY**

In view of the above remarks, new claims 44-83 are in condition for allowance. Applicant respectfully requests reconsideration, withdrawal of the outstanding rejection, and notifications of allowance. Should the Examiner have any questions or suggestions regarding the prosecution of this application, he is asked to contact applicant's representative at the telephone number listed below.

Respectfully submitted,



Philip H. Schlazer

Reg. No. 42,127

Date: 10 September 2001  
Energy Conversion Devices  
2956 Waterview  
Rochester Hills, MI 48309

Phone (248) 293-0440 extension 6260  
Fax (248) 844-2273